CLAIMS

1. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said bit line contact feature is characterized by a contact hole bounded by insulating side walls; and

said contact hole is partially filled with a conductively doped polysilicon plug defining an upper plug surface profile at least a portion of which is substantially convex.

2. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said bit line contact feature is characterized by a contact hole bounded by insulating side walls; and

said contact hole is completely filled with a conductively doped polysilicon plug defining an upper plug surface profile at least a portion of which is substantially convex.

3. A memory cell array including a plurality of memory cells, each of said memory cells being defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and

one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said bit line contact feature is characterized by a contact hole bounded by insulating side walls; and

said contact hole is filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially free of concavities.

4. A computer system comprising a microprocessor in communication with a memory device including a memory cell array, said memory cell array including a plurality of memory cells, each of said memory cells being defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said bit line contact feature is characterized by a contact hole bounded by insulating side walls; and

said contact hole is filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially free of concavities.

5. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said word line space feature line feature is characterized by a contact hole bounded by insulating side walls;

said contact hole is filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially free of concavities; and

said memory cell further comprises a storage node coupled to said upper plug surface profile.

6. The memory cell of claim 5 wherein said contact hole is filled to less than the uppermost extent of said insulating sidewalls.

7. The memory cell of claim 5 wherein said contact hole is filled to at least the uppermost extent of said insulating sidewalls.

8. The memory cell of claim 5 wherein said insulating side walls comprise a first pair of opposing insulating side walls along said first dimension and a second pair of opposing insulating side walls along said second dimension.

9. The memory cell of claim 8 wherein said first pair of opposing insulating sidewalls comprise respective layers of insulating spacer material formed over a conductive line.

10. (Amended) The memory cell of claim 8 wherein said second pair of opposing insulating side walls comprise respective layers of insulating material formed between respective contact holes.

11. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and

one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said word line space feature line feature is characterized by a contact hole bounded by insulating side walls;

said contact hole is partially filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially free of concavities; and

said memory cell further comprises a storage node coupled to said upper plug surface profile.

12. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said word line space feature line feature is characterized by a contact hole bounded by insulating side walls;

said contact hole is completely filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially free of concavities; and

said memory cell further comprises a storage node coupled to said upper plug surface profile.

13. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said word line space feature line feature is characterized by a contact hole bounded by insulating side walls;

said contact hole is partially filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially convex; and

said memory cell further comprises a storage node coupled to said upper plug surface profile.

14. A memory cell defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said word line space feature line feature is characterized by a contact hole bounded by insulating side walls;

said contact hole is completely filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially convex; and

said memory cell further comprises a storage node coupled to said upper plug surface profile.

15. A memory cell array including a plurality of memory cells, each of said memory cells being defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said word line space feature line feature is characterized by a contact hole bounded by insulating side walls;

said contact hole is filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially free of concavities; and

said memory cell further comprises a storage node coupled to said upper plug surface profile.

16. A computer system comprising a microprocessor in communication with a memory device including a memory cell array, said memory cell array including a plurality of memory cells, each of said memory cells being defined along first and second orthogonal dimensions wherein:

said first dimension is characterized by one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

said second dimension is characterized by two one-half field oxide features and one active area feature;

said first and second dimensions define a $6F^2$ memory cell;

said word line space feature line feature is characterized by a contact hole bounded by insulating side walls;

said contact hole is filled with a conductively doped polysilicon plug defining an upper plug surface profile that is substantially free of concavities; and

said memory cell further comprises a storage node coupled to said upper plug surface profile.

17. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a contact hole; and

said doped polysilicon plug defines an upper plug surface profile that is substantially free of concavities and is in contact with said bit line.

18. The memory cell of claim 17 wherein said polysilicon plug completely fills said contact hole.

19. The memory cell of claim 17 wherein said polysilicon plug partially fills said contact hole.

20. The memory cell of claim 17 wherein said insulating side walls comprise a first pair of opposing insulating side walls along said first dimension and a second pair of opposing insulating side walls along said second dimension.

21. The memory cell of claim 20 wherein said first pair of opposing insulating sidewalls comprise respective layers of insulating spacer material formed over a conductive line.

22. The memory cell of claim 20 wherein said second pair of opposing insulating side walls comprise respective layers of insulating material formed between respective contact holes.

23. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a contact hole;

said polysilicon plug partially fills said contact hole; and

said doped polysilicon plug defines an upper plug surface profile that is substantially convex and is in contact with said bit line.

24. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a contact hole;

said polysilicon plug completely fills said contact hole; and

said doped polysilicon plug defines an upper plug surface profile that is substantially convex and is in contact with said bit line.

25. A memory cell array comprising electrically conductive word lines and bit lines, an array of electrical charge storage structures, an array of transistor structures, and an array of bit line contacts, wherein:

each of said charge storage structures is conductively coupled to one of said bit lines via a selected transistor structure and a selected bit line contact;

each of said transistor structures is conductively coupled to one of said word lines;

each of said selected bit line contacts comprises a conductively doped polysilicon plug formed within a contact hole bounded by insulating side walls;

each of said doped polysilicon plugs define an upper plug surface profile that is substantially free of concavities and is in contact with an associated one of said bit lines.

26. A computer system comprising a microprocessor in communication with a memory device including a memory cell array, said memory cell array including electrically conductive word lines and bit lines, an array of electrical charge storage structures, an array of transistor structures, and an array of bit line contacts, wherein:

each of said charge storage structures is conductively coupled to one of said bit lines via a selected transistor structure and a selected bit line contact;

each of said transistor structures is conductively coupled to one of said word lines;

each of said selected bit line contacts comprises a conductively doped polysilicon plug formed within a contact hole bounded by insulating side walls;

each of said doped polysilicon plugs define an upper plug surface profile that is substantially free of concavities and is in contact with an associated one of said bit lines.

27. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a first contact hole bounded by insulating side walls;

said doped polysilicon plug defines an upper plug surface profile that is substantially free of concavities and is in contact with said bit line;

said charge storage structure further comprises a storage node including a conductively doped polysilicon plug formed within a second contact hole bounded by insulating side walls; and

said doped polysilicon plug of said storage node defines an upper plug surface profile that is substantially free of concavities.

28. The memory cell of claim 27 wherein said polysilicon plug completely fills said contact hole.

29. The memory cell of claim 27 wherein said polysilicon plug partially fills said contact hole.

30. The memory cell of claim 27 wherein said insulating side walls of said first contact hole comprise a first pair of opposing insulating side walls along said first dimension and a second pair of opposing insulating side walls along said second dimension.

31. The memory cell of claim 30 wherein said first pair of opposing insulating sidewalls comprise respective layers of insulating spacer material formed over a conductive line.

32. The memory cell of claim 30 wherein said second pair of opposing insulating side walls comprise respective layers of insulating material formed between respective contact holes.

33. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a first contact hole bounded by insulating side walls;

said polysilicon plug partially fills said first contact hole;

said doped polysilicon plug defines an upper plug surface profile that is substantially convex and is in contact with said bit line;

said charge storage structure further comprises a storage node including a conductively doped polysilicon plug formed within a second contact hole bounded by insulating side walls;

said polysilicon plug partially fills said second contact hole; and

said doped polysilicon plug of said storage node defines an upper plug surface profile that is substantially convex.

34. A memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, wherein:

said charge storage structure is conductively coupled to said bit line via said transistor structure and said bit line contact;

said transistor structure is conductively coupled to said word line;

said bit line contact comprises a conductively doped polysilicon plug formed within a first contact hole bounded by insulating side walls;

said polysilicon plug completely fills said first contact hole;

said doped polysilicon plug defines an upper plug surface profile that is substantially convex and is in contact with said bit line;

said charge storage structure further comprises a storage node including a conductively doped polysilicon plug formed within a second contact hole bounded by insulating side walls;

said polysilicon plug completely fills said second contact hole; and

said doped polysilicon plug of said storage node defines an upper plug surface profile that is substantially convex.

35. A memory cell array comprising electrically conductive word lines and bit lines, an array of electrical charge storage structures, an array of transistor structures, and an array of bit line contacts, wherein:

each of said charge storage structures is conductively coupled to one of said bit lines via a selected transistor structure and a selected bit line contact;

each of said transistor structures is conductively coupled to one of said word lines;

each of said selected bit line contacts comprises a conductively doped polysilicon plug formed within a first contact hole bounded by insulating side walls;

each of said doped polysilicon plugs define an upper plug surface profile that is substantially free of concavities and is in contact with an associated one of said bit lines;

each of said charge storage structures further comprises a storage node including a conductively doped polysilicon plug formed within a second contact hole bounded by insulating side walls; and

said doped polysilicon plug of said storage node define an upper plug surface profile that is substantially free of concavities.

36. A computer system comprising a microprocessor in communication with a memory device including a memory cell array, said memory cell array including electrically conductive word lines and bit lines, an array of electrical charge storage structures, an array of transistor structures, an an array of bit line contacts, wherein:

each of said charge storage structures is conductively coupled to one of said bit lines via a selected transistor structure and a selected bit line contact;

each of said transistor structures is conductively coupled to one of said word

lines;

each of said selected bit line contacts comprises a conductively doped polysilicon plug formed within a first contact hole bounded by insulating side walls;

each of said doped polysilicon plugs define an upper plug surface profile that is substantially free of concavities in contact with said bit line;

each of said charge storage structure further comprises a storage node including a conductively doped polysilicon plug formed within a second contact hole bounded by insulating side walls; and

said doped polysilicon plug of said storage node define an upper plug surface profile that is substantially free of concavities.

37. A memory device comprising:

a substrate having a first active area formed therein;

at least one insulating layer over said substrate;

a bitline over said at least one insulating layer;

a bitline contact configured to couple said bitline to said active area, said bitline contact characterized by:

a contact hole formed through said at least one insulating layer, said at least one insulating layer defining insulating sidewalls; and,

a conductive plug formed within said contact hole, said conductive plug having an upper plug surface profile free of significant concavities, wherein at least said upper plug surface profile is defined by a doped polysilicon.

38. The memory device of claim 37 wherein said conductive plug comprises a conductive material deposited so as to fill said contact hole, wherein said conductive material is etched back and a selective doped polysilicon is grown thereon defining said upper plug surface profile.

39. The memory device of claim 37 wherein said conductive plug comprises a conductive material deposited so as to partially fill said contact hole and a selective doped polysilicon is grown thereon defining said upper plug surface profile.

40. The memory device of claim 37 wherein said conductive plug completely fills said contact hole.

41. The memory device of claim 37 wherein said conductive plug partially fills said contact hole.

42. A semiconductor device comprising:

a substrate having a first active area formed therein;

at least one insulating layer over said substrate;

a conductive line over said at least one insulating layer;

a contact configured to couple said conductive line to said active area, said contact characterized by:

a contact hole formed through said at least one insulating layer, said at least one insulating layer defining insulating sidewalls; and,

a conductive plug formed within said contact hole, said conductive plug having a substantially convex upper plug surface profile, wherein at least said upper plug surface profile is defined by a doped polysilicon, and wherein said conductive plug completely fills said contact hole.

43. A semiconductor device comprising:

a substrate having a first active area formed therein;

at least one insulating layer over said substrate;

a conductive line over said at least one insulating layer;

a contact configured to couple said conductive line to said active area, said

contact characterized by:

a contact hole formed through said at least one insulating layer, said at least one insulating layer defining insulating sidewalls; and,

a conductive plug formed within said contact hole, said conductive plug having a substantially convex upper plug surface profile, wherein at least said upper plug surface profile is defined by a doped polysilicon, and wherein said conductive plug partially fills said contact hole.

44. A semiconductor device comprising:

a substrate having a first active area formed therein;

at least one insulating layer over said substrate;

a capacitor over said at least one insulating layer;

a contact configured to couple said capacitor to said active area, said contact characterized by:

a contact hole formed through said at least one insulating layer, said at least one insulating layer defining insulating sidewalls; and,

a conductive plug formed within said contact hole, said conductive plug having an upper plug surface profile free of significant concavities, wherein at least said upper plug surface profile is defined by a doped polysilicon.